Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

1. (Original) A phase comparator, comprising:

a phase detector having a first input for receiving a first signal, a second input for receiving a second signal, and an output for providing an error signal indicative of a phase relationship between the first signal and the second signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal.

2. (Original) The phase comparator of claim 1, wherein the phase detector is a two-state phase detector and wherein the error signal has a first logic state indicative of a phase error between the first signal and the second signal.

3. (Original) The phase comparator of claim 2, wherein the two-state phase detector is an XOR logic gate.

4. (Original) The phase comparator of claim 2, wherein the two-state phase detector is a two-state sequential phase detector.

5. (Original) The phase comparator of claim 1, wherein the phase detector is a three-state phase detector and wherein the error signal has a first output indicative of phase lead between the first signal and the second signal, and a second output indicative of phase lag between the first signal and the second signal.

A1

6. (Original) The phase comparator of claim 1, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

7. (Original) The phase comparator of claim 1, wherein the sampling clock signal has a frequency that is within 10% of a target frequency, wherein the target frequency is substantially matched to a resolution of the digital-to-analog converter.

8. (Original) The phase comparator of claim 1, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital counter.

9. (Original) The phase comparator of claim 1, wherein the digital counter has a resolution that matches or exceeds a resolution of the digital-to-analog converter.

10. (Original) A phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving a first reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal;

a filter having an input for receiving the error voltage signal and an output for providing a control voltage signal; and

a voltage-controlled oscillator having an input for receiving the control voltage signal and an output for providing an output signal, wherein the feedback signal is derived from the output signal.

A1

11. (Original) The phase locked loop of claim 10, wherein the phase detector is a two-state phase detector.

12. (Original) The phase locked loop of claim 11, wherein the two-state phase detector is an XOR logic gate.

13. (Original) The phase locked loop of claim 11, wherein the two-state phase detector is a two-state sequential phase detector.

14. (Original) The phase locked loop of claim 10, wherein the phase detector is a three-state phase/frequency phase detector.

15. (Original) The phase locked loop of claim 10, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

16. (Original) The phase locked loop of claim 10, wherein the sampling clock signal has a frequency that is within 10% of a target frequency, wherein the target frequency is substantially matched to a resolution of the digital-to-analog converter.

17. (Original) The phase locked loop of claim 10, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital counter.

18. (Original) The phase locked loop of claim 10 wherein the digital counter has a resolution that matches or exceeds a resolution of the digital-to-analog converter.

19. (Original) The phase locked loop of claim 10 wherein the filter further comprises an active filter.

A1

20. (Original) The phase locked loop of claim 10 wherein the voltage-controlled oscillator is a voltage-controlled crystal oscillator.

21. (Original) The phase locked loop of claim 10 wherein the feedback signal is the output signal of the voltage-controlled oscillator.

22. (Original) The phase locked loop of claim 10 further comprising a frequency divider coupled between the output of the voltage-controlled oscillator and the second input of the phase detector, wherein the frequency divider comprises a divide-by-N block and wherein a target frequency of the output signal of the voltage-controlled oscillator is approximately N times a frequency of the first reference clock signal.

23. (Original) The phase locked loop of claim 10 further comprising:

a frequency divider having an input for receiving a second reference clock signal and an output for providing the first reference clock signal as a selected fraction of the second reference clock signal.

24. (Original) The phase locked loop of claim 23, wherein the frequency divider comprises a divide-by-two block, thereby producing a first reference clock signal having a 50% duty cycle and a frequency of approximately one-half of a frequency of the second reference clock signal.

25. (Original) A shelf controller for controlling synchronization of shelf elements in a communications network element, the shelf controller comprising:

a processor; and

a timing circuit coupled to the processor, wherein the timing circuit comprises:

a phase locked loop, comprising:

a phase comparator, comprising:

A1

a phase detector having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal;

a filter having an input for receiving the error voltage signal and an output for providing a control voltage signal; and

a voltage-controlled oscillator having an input for receiving the control voltage signal and an output for providing a synchronization timing signal for the synchronization of the shelf elements, wherein the feedback signal is derived from the output of the voltage-controlled oscillator.

26. (Original) A method of generating a timing signal, comprising:

generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal;

generating a count value indicative of an amount of phase error during a single event;

generating an error voltage signal proportional to the count value;

filtering the error voltage signal to produce a control voltage signal;

generating the timing signal in response to the control voltage signal; and

deriving the feedback signal from the timing signal.

27. (Original) The method of claim 26, wherein generating an error signal comprises generating an error signal with a two-state phase detector and wherein the single event comprises a single period of the error signal.

A1

28. (Original) The method of claim 27, wherein generating a count value comprises incrementing a digital counter in response to a sampling clock signal during a time when the error signal has a first logic state and wherein generating an error voltage occurs at a time when the error signal transitions from the first logic state to a second logic state.

29. (Original) The method of claim 26, wherein generating the timing signal comprises applying the control voltage to a voltage-controlled oscillator.

30. (Original) The method of claim 26, wherein deriving the feedback signal from the timing signal comprises dividing the feedback signal by a selected factor N, wherein the timing signal has a target frequency of approximately N times a frequency of the reference clock signal.

31. (Original) A method of generating a timing signal, comprising:

generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal, wherein the error signal has a first logic state indicative of phase error between the reference clock signal and the feedback signal and a second logic state indicative of the reference clock signal and the feedback signal sharing the same phase state;

generating a count value indicative of an amount of phase error during a single period of the error signal;

generating an error voltage signal proportional to the count value;

filtering the error voltage signal to produce a control voltage signal;

generating the timing signal in response to the control voltage signal; and

deriving the feedback signal from the timing signal.

32. (Original) A network element for a communications network, the network element comprising:

a shelf backplane; and

A1

a plurality of shelf elements coupled to the shelf backplane, wherein the plurality of shelf elements includes at least one shelf controller for controlling synchronization of the plurality of shelf elements, the at least one shelf controller comprising:

a processor; and

a timing circuit coupled to the processor, wherein the timing circuit comprises:

a phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal;

a filter having an input for receiving the error voltage signal and an output for providing a control voltage signal; and

a voltage-controlled oscillator having an input for receiving the control voltage signal and an output;

wherein the timing circuit provides a synchronization timing signal to the shelf backplane for the synchronization of the plurality of shelf elements; and

wherein the synchronization timing signal is derived from the output of the voltage-controlled oscillator.

33. (Original) A phase locked loop, comprising:

A1

a first frequency divider having an input for receiving a first reference clock signal and an output for providing a second reference clock signal;

a phase comparator, comprising:

a two-state phase detector having a first input for receiving the second reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal indicative of a phase relationship between the second reference clock signal and the feedback signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value, wherein the count value is indicative of an amount of phase error during a single period of the error signal; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal proportional to the count value;

an active filter having an input for receiving the error voltage signal and an output for providing a control voltage signal, wherein the control voltage signal is representative of an average value of the error voltage signal during a period of time;

a voltage-controlled oscillator having an input for receiving the control voltage signal and an output for providing an output signal, wherein the output signal is an oscillating signal proportional to the control voltage signal; and

a second frequency divider having an input for receiving the output signal and an output for providing the feedback signal, wherein the feedback signal has a frequency approaching a frequency of the second reference clock signal.

34. (Original) The phase locked loop of claim 33, wherein the two-state phase detector is an XOR logic gate.

35. (Original) The phase locked loop of claim 33, wherein the two-state phase detector is a two-state sequential phase detector.

36. (Original) The phase locked loop of claim 33, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

37. (Original) The phase locked loop of claim 33, wherein the voltage-controlled oscillator is a voltage-controlled crystal oscillator.

38. (Original) The phase locked loop of claim 33, wherein the first frequency divider comprises a divide-by-two block, thereby producing the second reference clock signal having a 50% duty cycle and a frequency of approximately one-half of a frequency of the first reference clock signal.

39. (Original) The phase locked loop of claim 38, wherein the output signal of the voltage-controlled oscillator has a frequency that is a selected multiple N of the frequency of the first reference clock signal, and wherein the second frequency divider comprises a divide-by-N block followed by a divide-by-two block, thereby producing the feedback signal having a 50% duty cycle and a frequency approaching the frequency of the second reference clock signal.

40. (Original) A method of generating a timing signal, comprising:

frequency dividing a first reference clock signal by a factor of two, thereby producing a second reference clock signal having a duty cycle of approximately 50% and a frequency of approximately one-half a frequency of the first reference clock signal;

generating an error signal indicative of a phase relationship between the second reference clock signal and a feedback signal using a two-state phase detector;

generating a count value indicative of an amount of phase error during a single period of the error signal by incrementing a digital counter in response to a sampling clock signal during a time when the error signal has a first logic state;

passing the count value to a digital-to-analog converter at a time when the error signal transitions from the first logic state to a second logic state;

resetting the digital counter to a selected initial value subsequent to passing the count value;

generating an error voltage signal proportional to the count value using the digital-to-analog converter;

filtering the error voltage signal using an active filter to produce a control voltage signal representative of an amplified average error voltage signal;

supplying the control voltage signal to a voltage-controlled oscillator to generate the timing signal; and

frequency dividing the timing signal to derive the feedback signal.

41. (Original) The method of claim 40, wherein frequency dividing the timing signal comprises first dividing the timing signal by a selected factor N, wherein the timing signal has a target frequency of approximately N times a frequency of the first reference clock signal, then dividing the resulting signal by a factor of two, thereby producing a feedback signal having a duty cycle of approximately 50% and a frequency approaching the frequency of the second reference clock signal.

42. (Original) A shelf controller for controlling synchronization of shelf elements in a communications network element, the shelf controller comprising:

a processor; and

a timing circuit coupled to the processor, wherein the timing circuit comprises:

a first phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving a first reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

A1

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal;

a filter having an input for receiving the error voltage signal and an output for providing a control voltage signal; and

a voltage-controlled oscillator having an input for receiving the control voltage signal and an output for providing a second reference clock signal, wherein the feedback signal is derived from the second reference clock signal; and

a second phase locked loop having an input for receiving the second reference clock signal and an output for providing a synchronization timing signal for the synchronization of the shelf elements, wherein the synchronization timing signal is derived from the second reference clock signal.

43. (Original) A method of generating a timing signal, comprising:

generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal using a three-state phase detector, wherein the error signal includes an up output and a down output;

generating a count value indicative of an amount of phase error during a single event, wherein the single event is a period between a rising edge of the reference clock signal and a next rising edge of the feedback signal when the up output is indicative of phase lead between the reference clock signal and the feedback signal and wherein the single event is a period between a rising edge of the feedback signal and a next rising edge of the reference clock signal when the down output is indicative of phase lag between the reference clock signal and the feedback signal;

generating an error voltage signal proportional to the count value;

filtering the error voltage signal to produce a control voltage signal;

A1

generating the timing signal in response to the control voltage signal; and
deriving the feedback signal from the timing signal.

44. (Original) The method of claim 43, wherein generating a count value indicative of an amount of phase error further comprises setting a digital counter to an initial value and incrementing the digital counter in response to a sampling clock signal during the single event when the up output is indicative of phase lead between the reference clock signal and the feedback signal and setting the digital counter to the initial value and decrementing the digital counter in response to the sampling clock signal during the single event when the down output is indicative of phase lag between the reference clock signal and the feedback signal.

45. (Original) A network element for a communications network, the network element comprising:

a shelf backplane; and

a plurality of shelf elements coupled to the shelf backplane, wherein the plurality of shelf elements includes at least one shelf controller for controlling synchronization of the plurality of shelf elements, the at least one shelf controller comprising:

a processor; and

a timing circuit coupled to the processor, wherein the timing circuit comprises:

a framer having an input for receiving recovered clock and data signals of a communication signal and an output for providing a first reference clock signal;

a first phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving the first reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal;

a filter having an input for receiving the error voltage signal and an output for providing a control voltage signal; and

a voltage-controlled oscillator having an input for receiving the control voltage signal and an output for providing a second reference clock signal, wherein the feedback signal is derived from the second reference clock signal; and

a second phase locked loop having an input for receiving the second reference clock signal and an output for providing a synchronization timing signal to the shelf backplane for the synchronization of the plurality of shelf elements, wherein the synchronization timing signal is derived from the second reference clock signal.

46. (New) The shelf controller of claim 25, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

47. (New) The shelf controller of claim 25, wherein the sampling clock signal has a frequency that is within 10% of a target frequency, wherein the target frequency is substantially matched to a resolution of the digital-to-analog converter.

48. (New) The shelf controller of claim 25, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital counter.

49. (New) The shelf controller of claim 25 wherein the digital counter has a resolution that matches or exceeds a resolution of the digital-to-analog converter.

50. (New) The network element of claim 32, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

51. (New) The network element of claim 32, wherein the sampling clock signal has a frequency that is within 10% of a target frequency, wherein the target frequency is substantially matched to a resolution of the digital-to-analog converter.

52. (New) The network element of claim 32, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital counter.

53. (New) The network element of claim 32 wherein the digital counter has a resolution that matches or exceeds a resolution of the digital-to-analog converter.

54. (New) The shelf controller of claim 42, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

55. (New) The shelf controller of claim 42, wherein the sampling clock signal has a frequency that is within 10% of a target frequency, wherein the target frequency is substantially matched to a resolution of the digital-to-analog converter.

56. (New) The shelf controller of claim 42, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital counter.

57. (New) The shelf controller of claim 42 wherein the digital counter has a resolution that matches or exceeds a resolution of the digital-to-analog converter.

58. (New) The network element of claim 45, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital-to-analog converter.

59. (New) The network element of claim 45, wherein the sampling clock signal has a frequency that is within 10% of a target frequency, wherein the target frequency is substantially matched to a resolution of the digital-to-analog converter.

60. (New) The network element of claim 45, wherein the sampling clock signal has a frequency that is substantially matched to a resolution of the digital counter.

61. (New) The network element of claim 45 wherein the digital counter has a resolution that matches or exceeds a resolution of the digital-to-analog converter.

62. (New) A shelf controller for controlling synchronization of shelf elements in a communications network element, the shelf controller comprising:

a processor; and

a timing circuit coupled to the processor, wherein the timing circuit comprises:

a phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal; and

a voltage-controlled oscillator having an input coupled to receive the error voltage signal and an output for providing a synchronization timing signal for the synchronization of the shelf elements, wherein the feedback signal is derived from the output of the voltage-controlled oscillator.

63. (New) A network element for a communications network, the network element comprising:

a shelf backplane; and

a plurality of shelf elements coupled to the shelf backplane, wherein the plurality of shelf elements includes at least one shelf controller for controlling synchronization of the plurality of shelf elements, the at least one shelf controller comprising:

a processor; and

a timing circuit coupled to the processor, wherein the timing circuit comprises:

a phase locked loop, comprising:

a phase comparator, comprising:

a phase detector having a first input for receiving a reference clock signal, a second input for receiving a feedback signal, and an output for providing an error signal;

a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal from the processor, and an output for providing a count value; and

a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal; and

a voltage-controlled oscillator having an input coupled to receive the error voltage signal and an output;

wherein the timing circuit provides a synchronization timing signal to the shelf backplane for the synchronization of the plurality of shelf elements; and

wherein the synchronization timing signal is derived from the output of the voltage-controlled oscillator.

64. (New) A method of generating a timing signal, comprising:

generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal;

adjusting a value of a counter a plurality of times during a single event to produce a value indicative of an amount of phase error during the single event;

generating an error voltage signal proportional to the count value;

generating the timing signal in response to the error voltage signal; and

deriving the feedback signal from the timing signal.

65. (New) The method of claim 64, wherein adjusting a value of the counter a plurality of times comprises adjusting the counter using a sampling clock signal.

66. (New) A method of generating a timing signal, comprising:

generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal;

generating a sampling clock signal to define a plurality of sampling intervals;

adjusting a value of a counter during sampling intervals for a single event based on the sampling clock to produce a value indicative of an amount of phase error during the single event;

generating an error voltage signal proportional to the count value;

generating the timing signal in response to the error voltage signal; and

deriving the feedback signal from the timing signal.